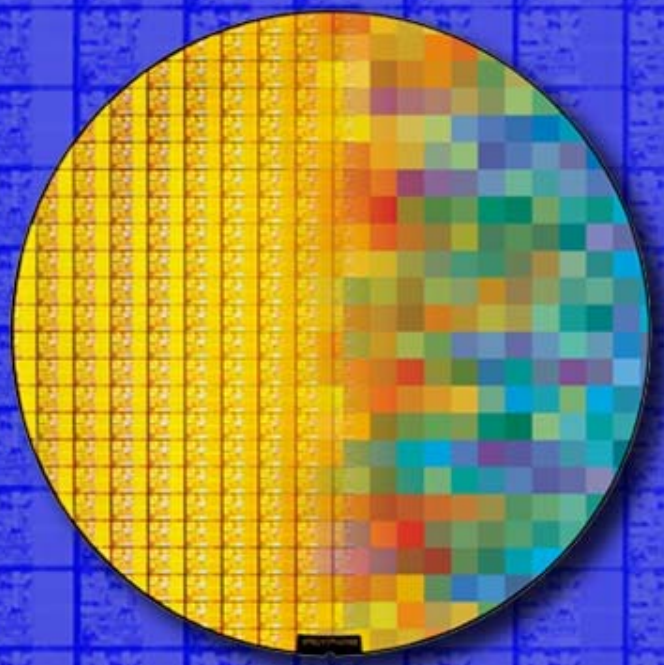


3D circuits & their test challenges

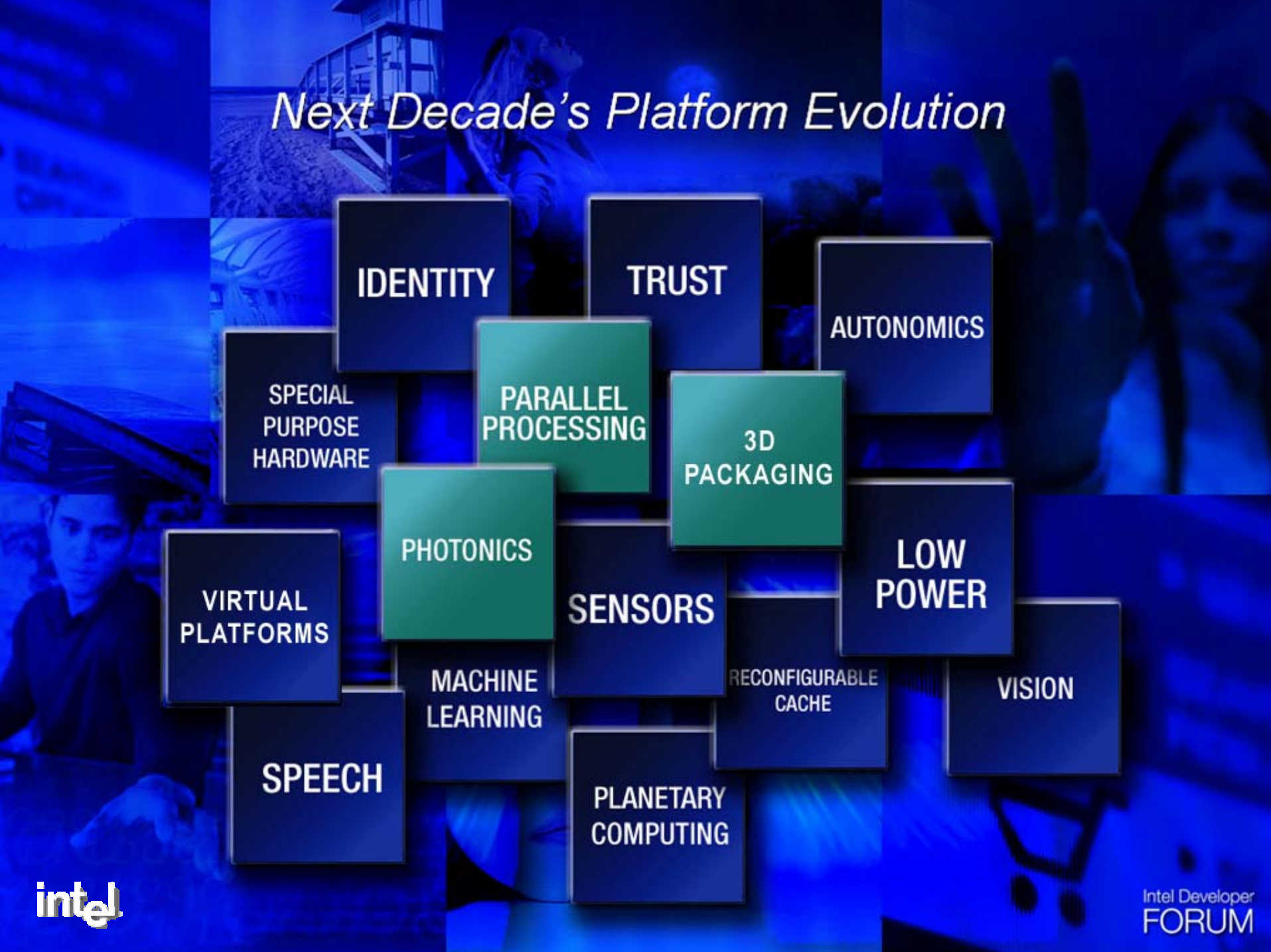
TM Mak

GSRC Technical Liaison
Test Technology

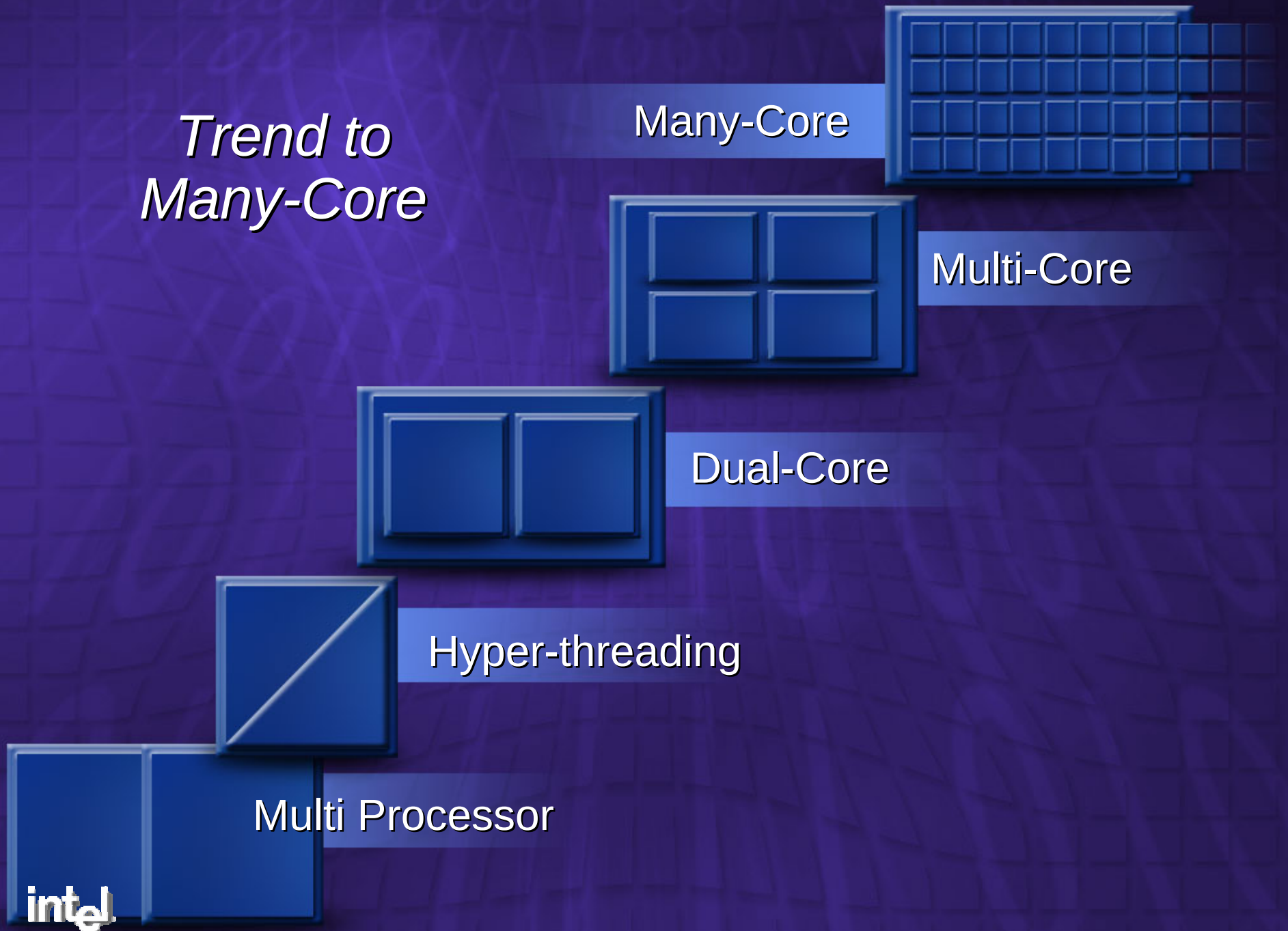
intel

What is new in computing?

Re: IDF Fall 2005

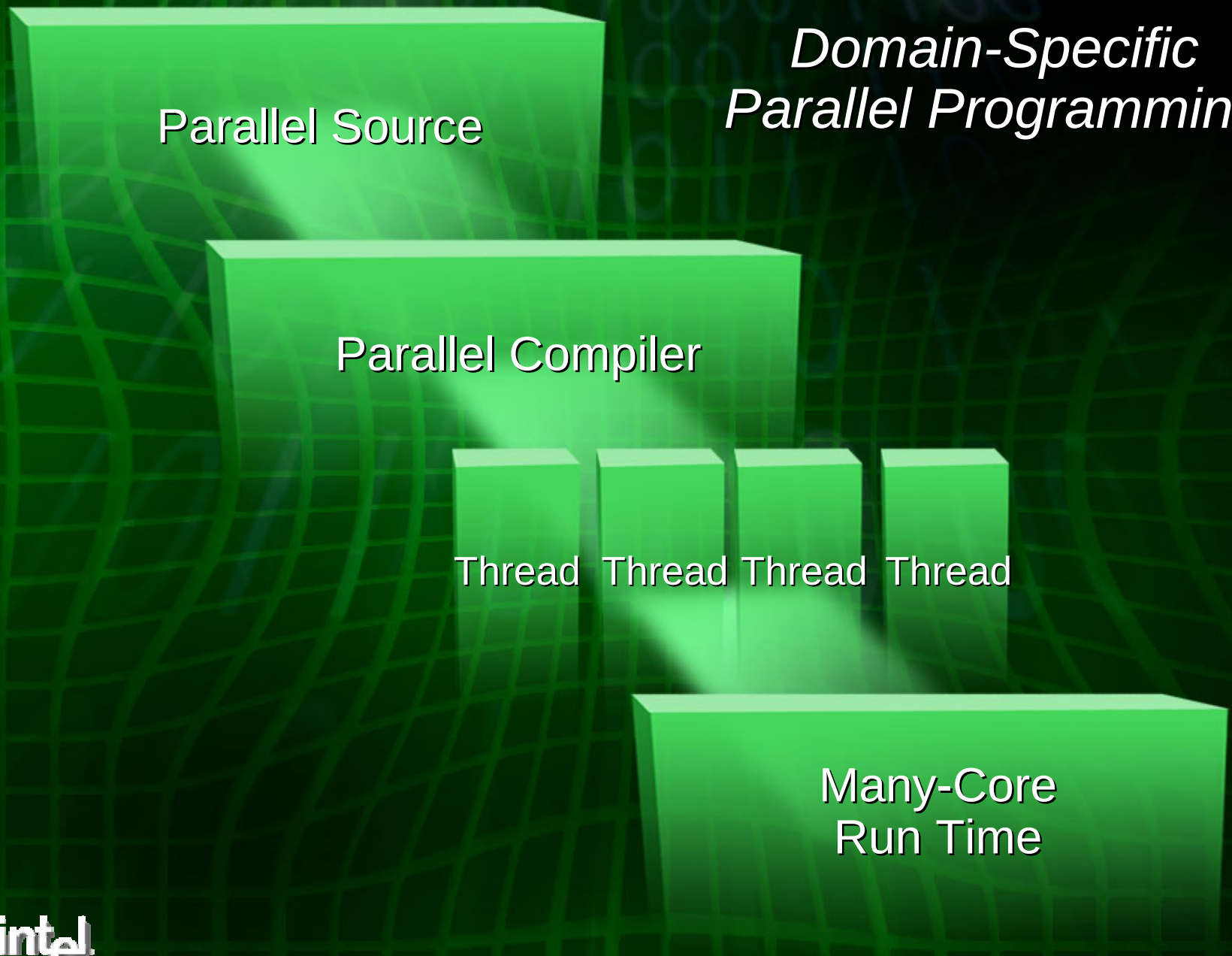

Next Decade's Platform Evolution
IDENTITY
TRUST
AUTONOMICS
SPECIAL PURPOSE HARDWARE
PARALLEL PROCESSING
3D PACKAGING
PHOTONICS
LOW POWER
VIRTUAL PLATFORMS
SENSORS
MACHINE LEARNING
RECONFIGURABLE CACHE
VISION
SPEECH
PLANETARY COMPUTING
intel
Intel Developer FORUM

Trend to Many-Core



Can you program it?

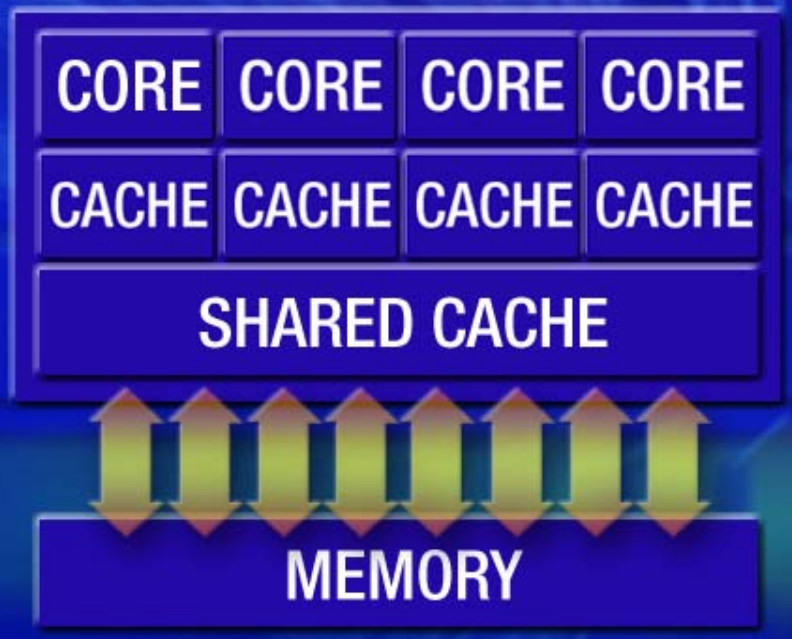
Can we feed it?

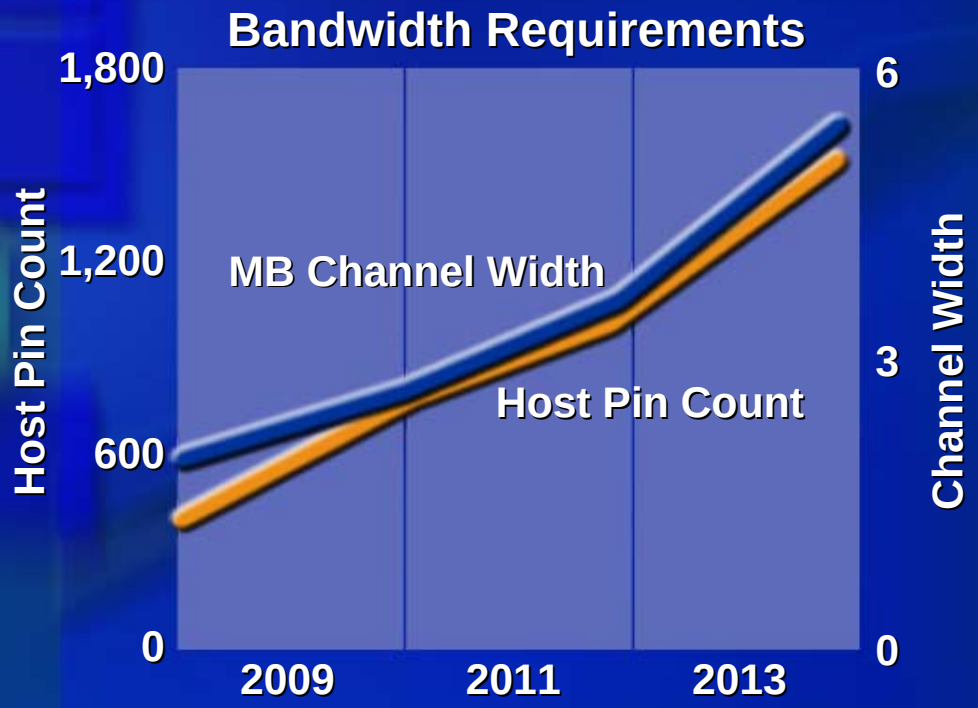

Parallel Source
Domain-Specific
Parallel Programming
Parallel Compiler
Thread
Thread
Thread
Thread
Many-Core
Run Time

Can you program it?

Can we feed it?

Memory Bandwidth Challenge





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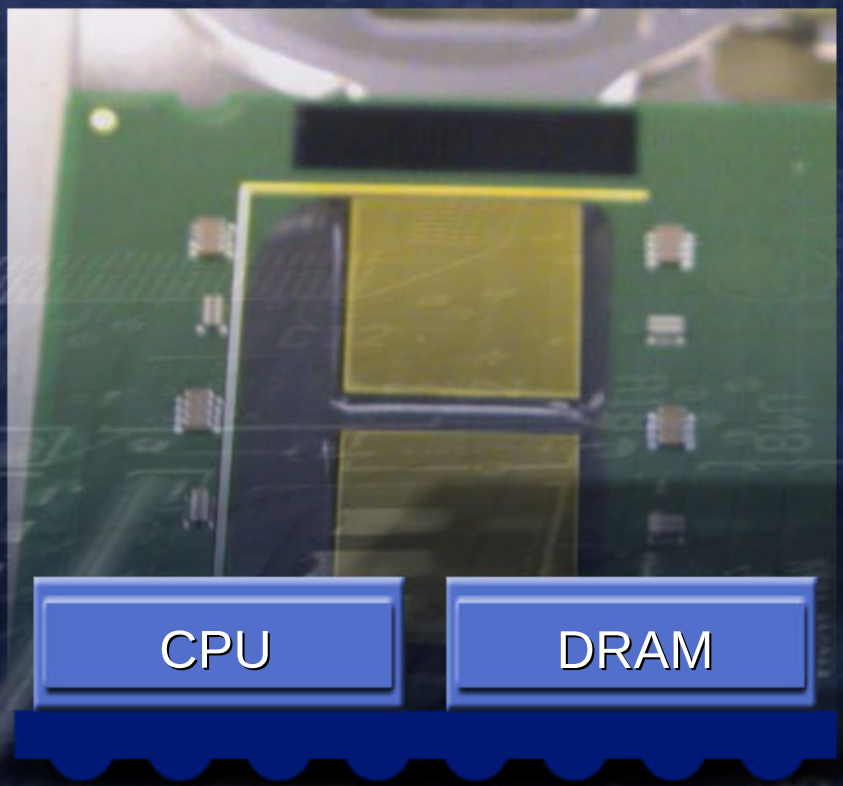
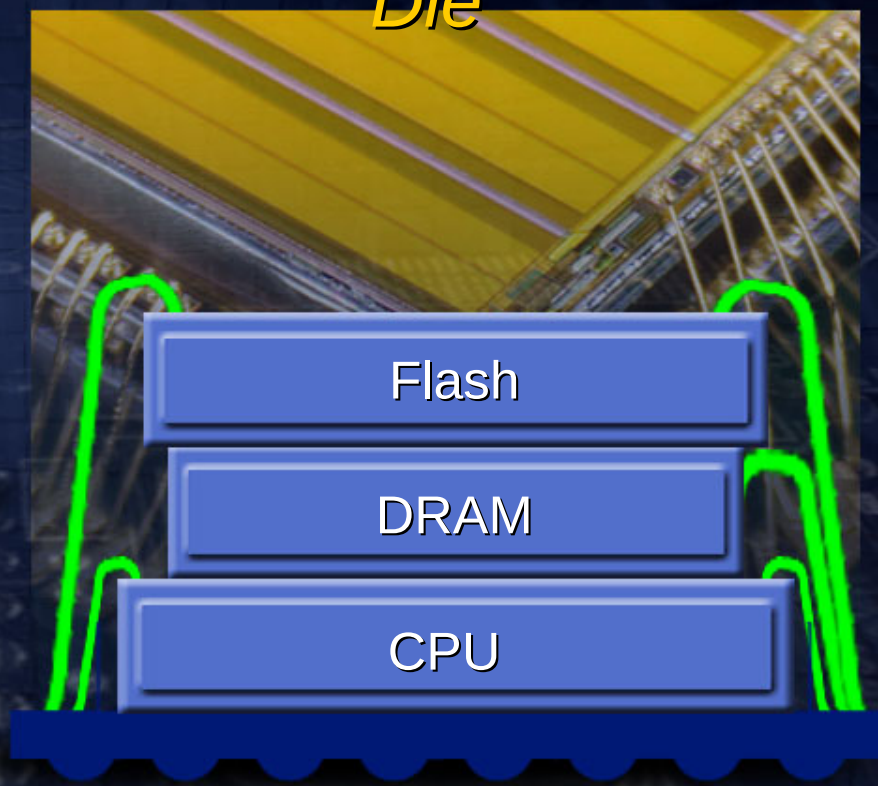
Today's Packaging Technology

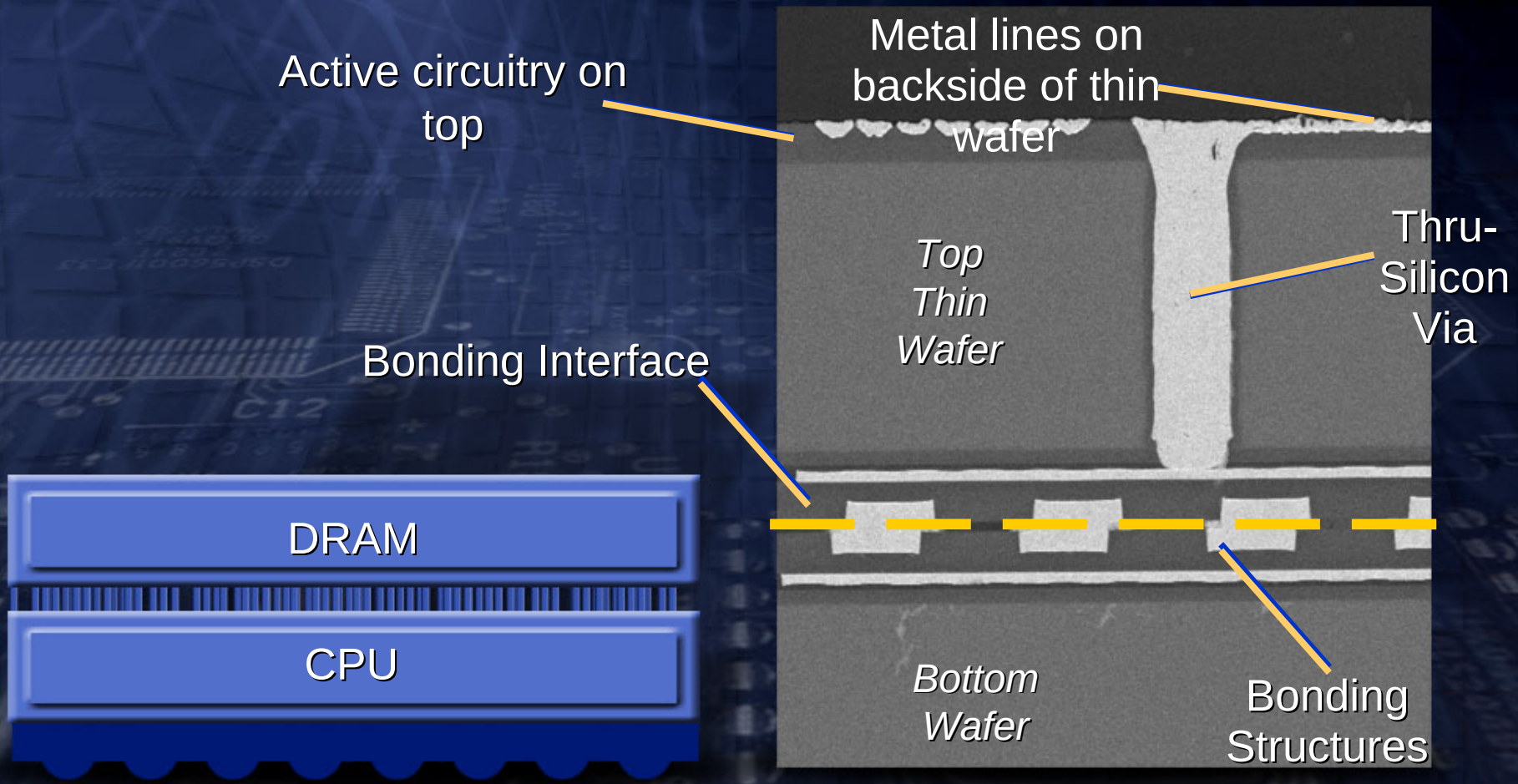
Multi-Chip Package



Wire-Bonded Stacked Die

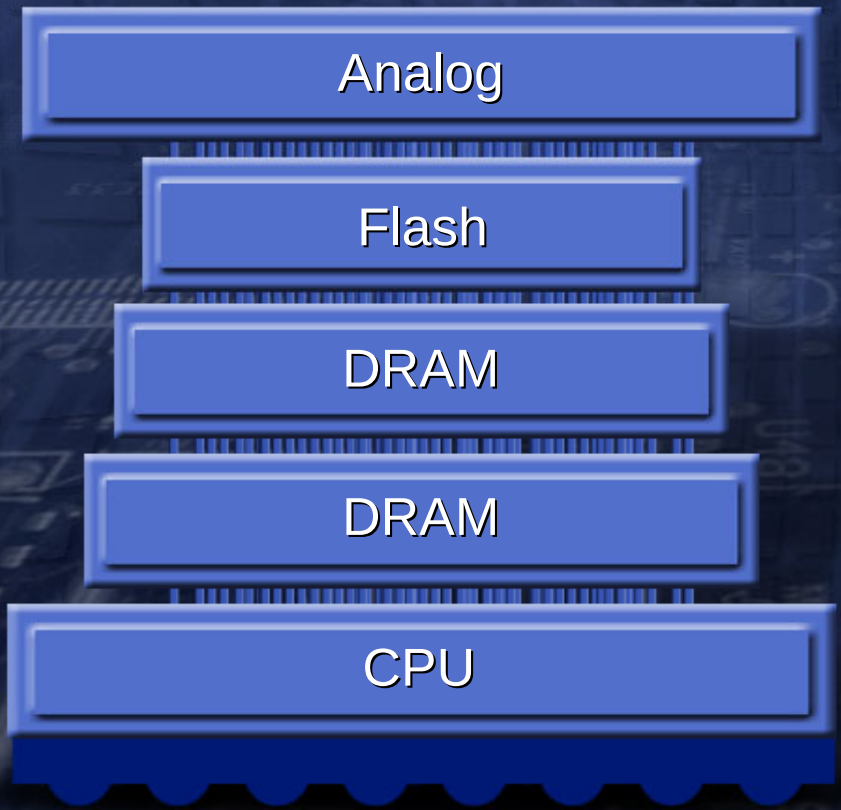


3D Stacking Research
Wafer Stacking



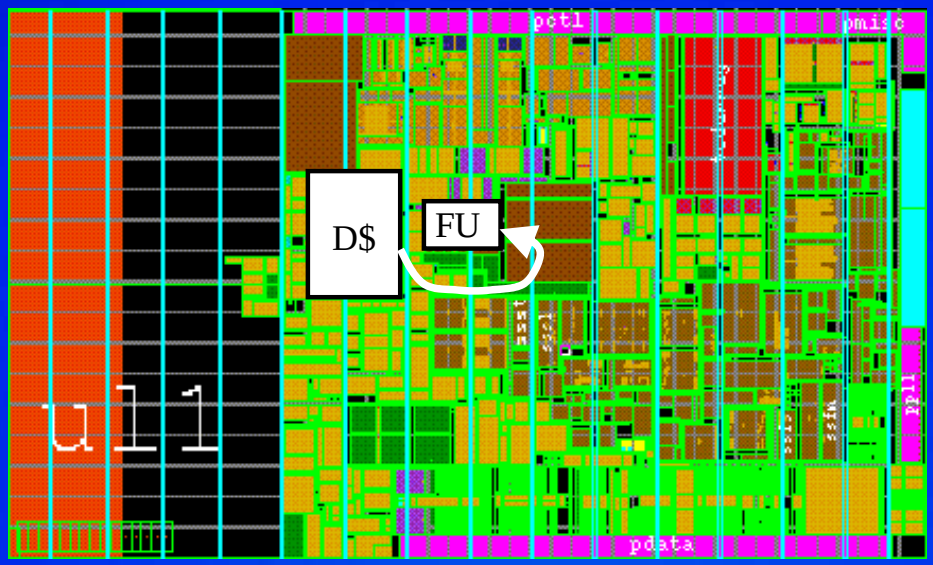
Source: Intel

3D Stacking Research
Die Stacking



Source: Intel

What about 3D for microprocessors?

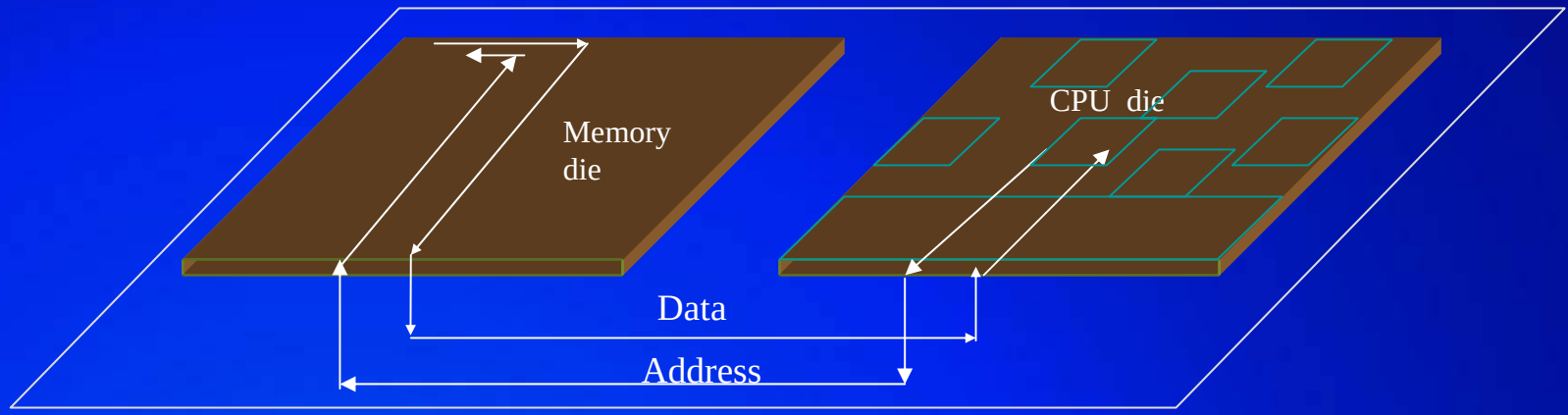


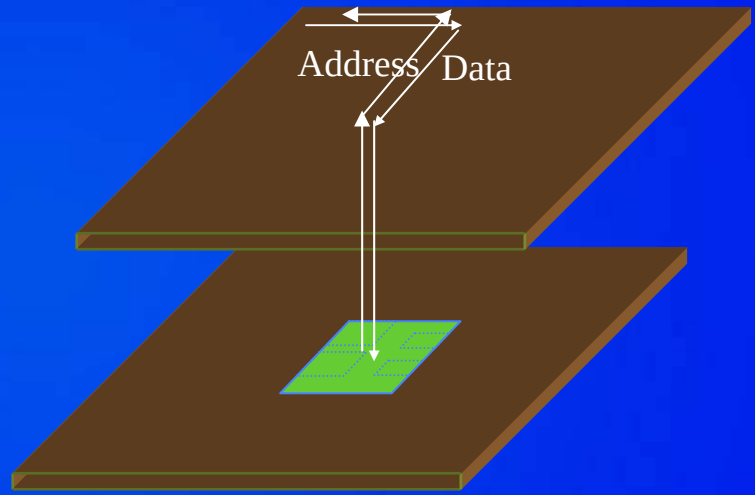
- Wiring is #2 limiter in chip level integration
  - 8 layers of metal
- Over half of performance loss is from wire delay
- Over half of power consumption is from wire capacitance
- Floorplan is a multivariate optimization exercise
  - Who wants to be next to whom?
  - Only 8 possible neighbors

Re: Back et. al., ICCAD04

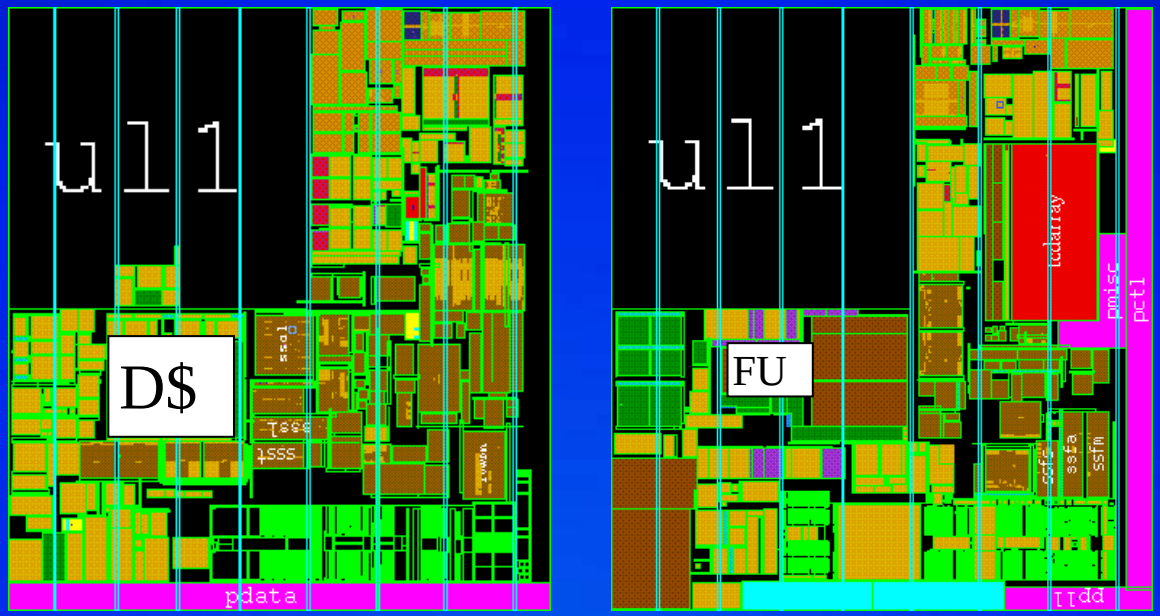
intel

Shorter Route, higher performance, lower power





Re-floorplan for 3D



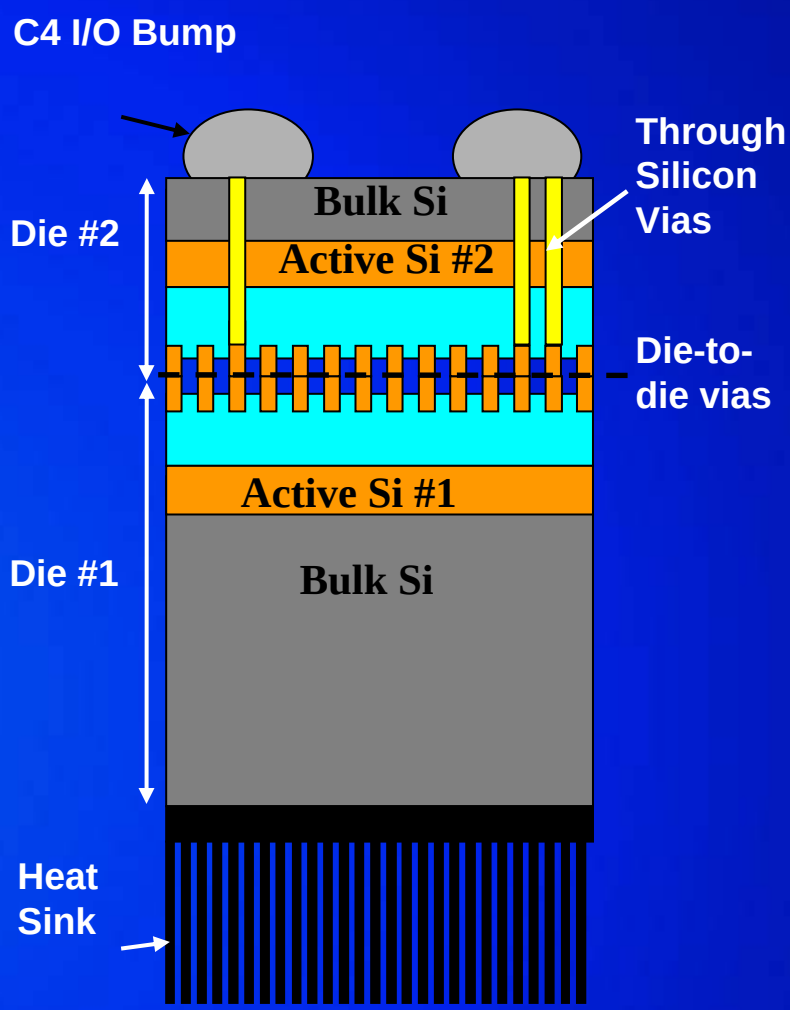
- Wires can be shortened to reduce wire delay and wireload
  - E.g. 50% less clock wires
- More flexibility for floorplanning
  - 2X more possible neighbor lots
- >15% Performance improvement
  - Pipe stage reduction
- 50% Less repeaters
- Caveats:
  - Avoid hot spot overlaps

Re: Back et. al., ICCAD04

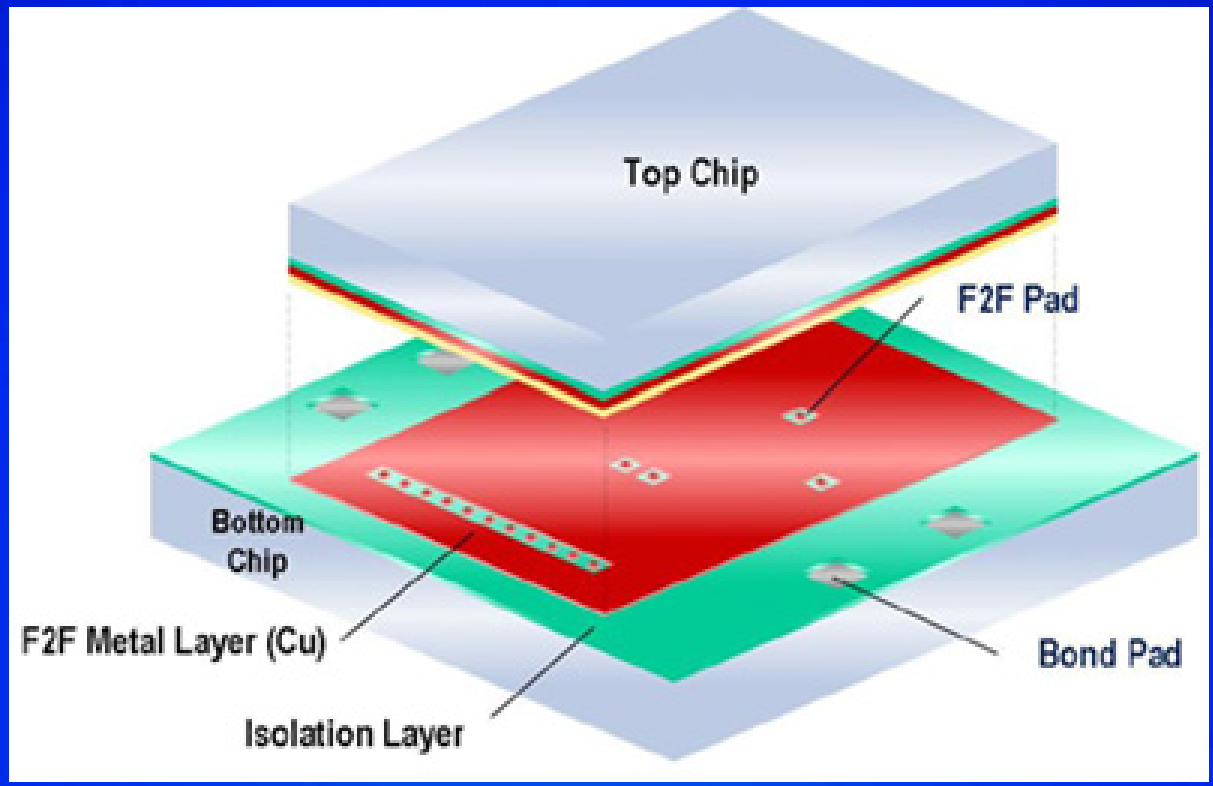
intel

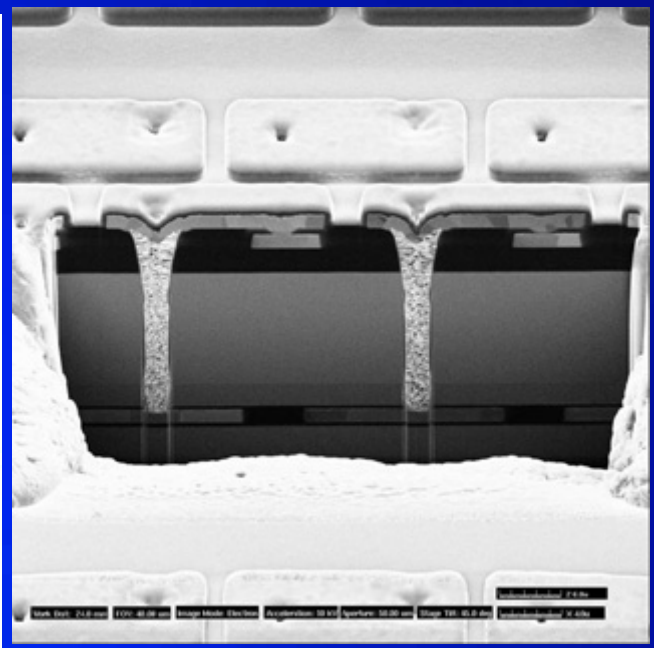
3D stack

- Face to face stacking
  - More die to die vias needed to facilitate the millions of connection between logic blocks



Face-to-Face (F2F) Stacking Process





Thru Silicon Via

(re: Fraunhofer Gesellschaft, IZM, Munich)

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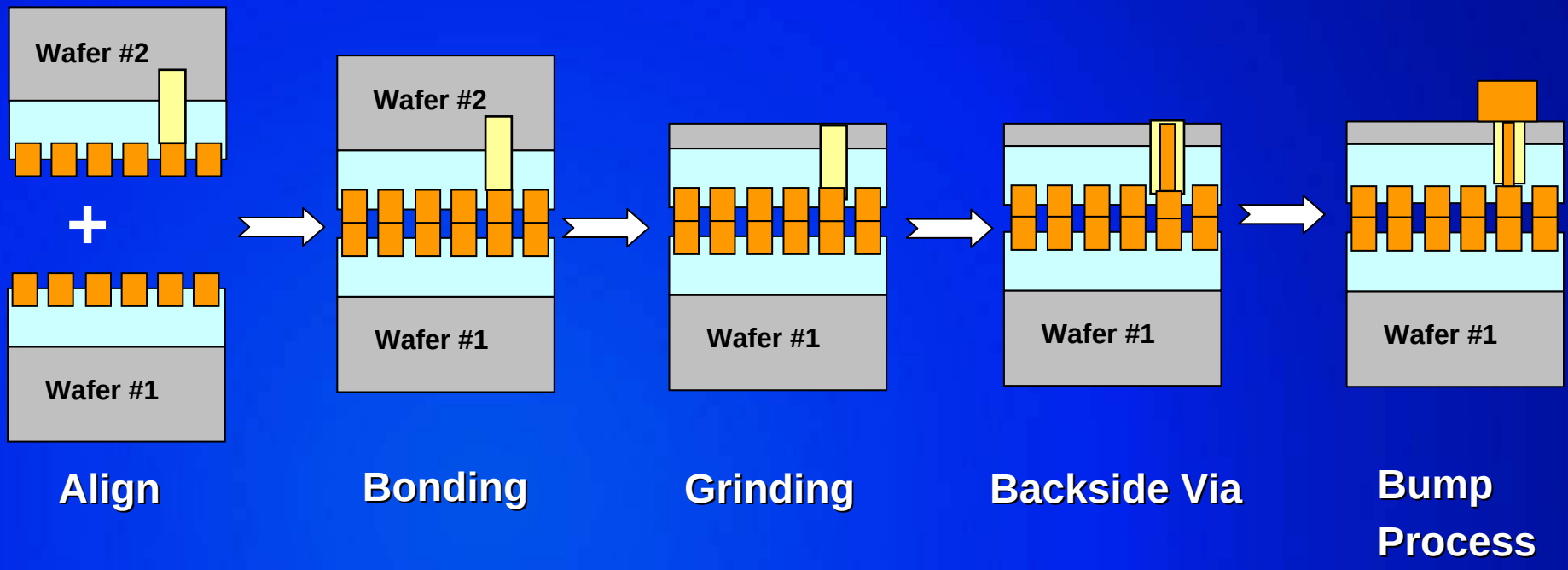
Build process (F2F stack)



Note buried via with wafer2

What does it mean to test?

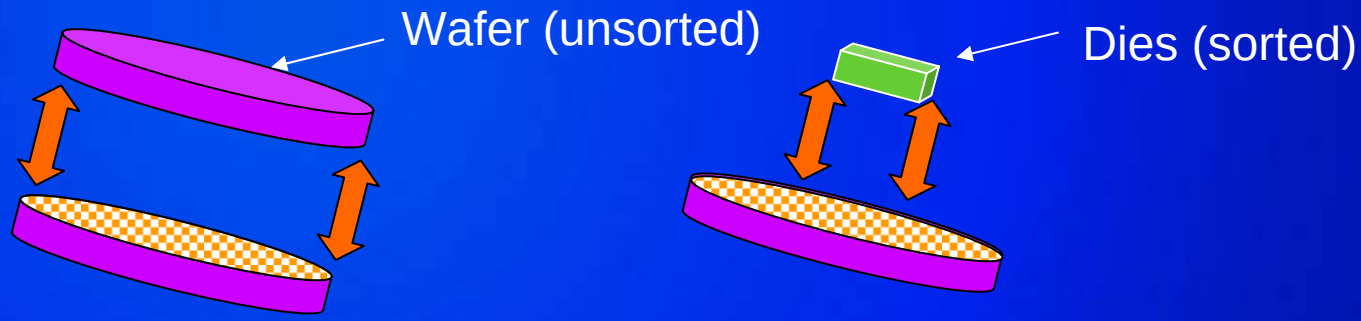
Die stack or wafer stack?

- Wafer stack (blind assembly) would lower yield drastically

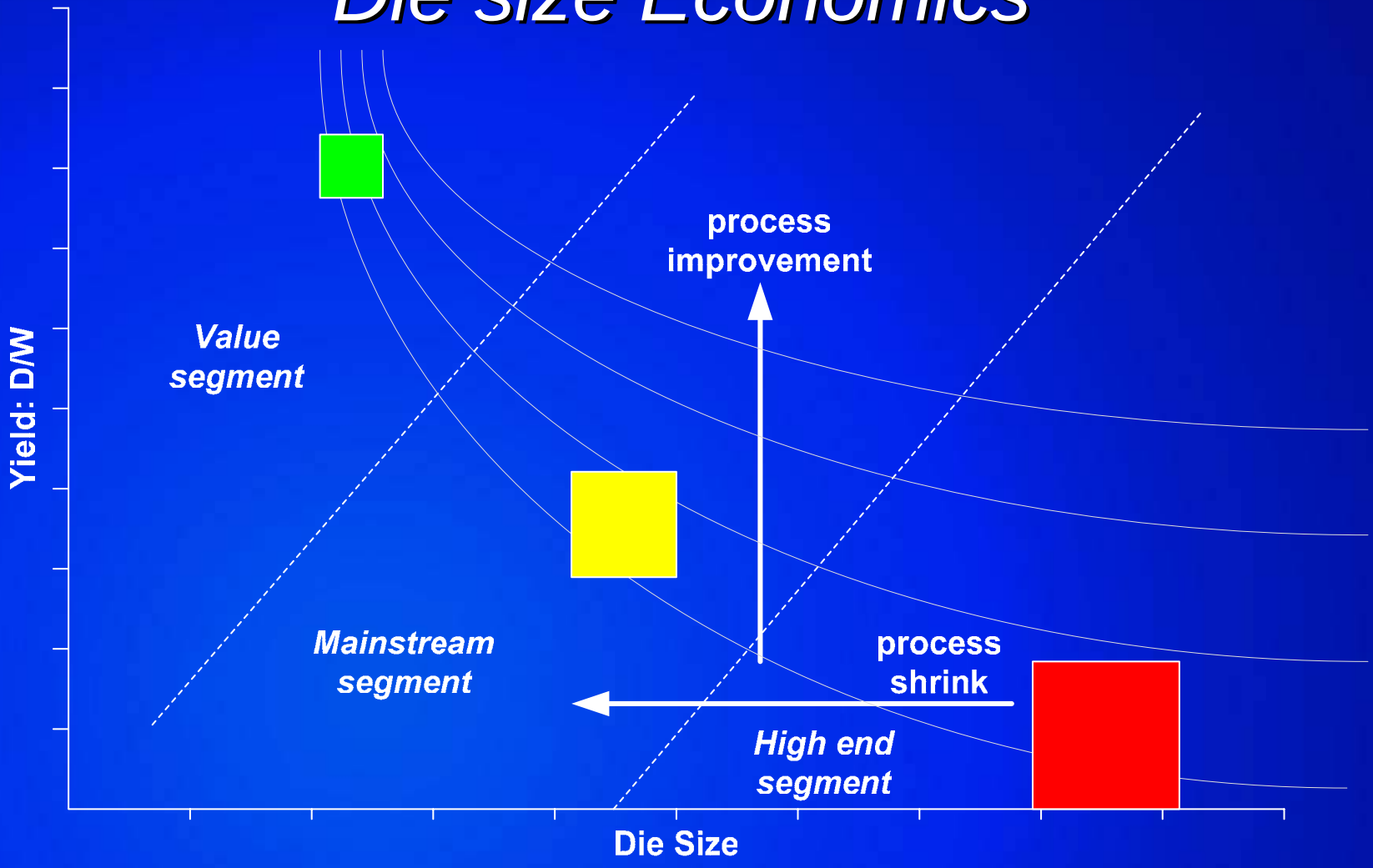
$$Y_{stack} = Y_{top} * Y_{bottom}$$

Note: this has not accounted for saving in pipestages or other wire/repeater reduction

- Die stacking allows better match of top and bottom die

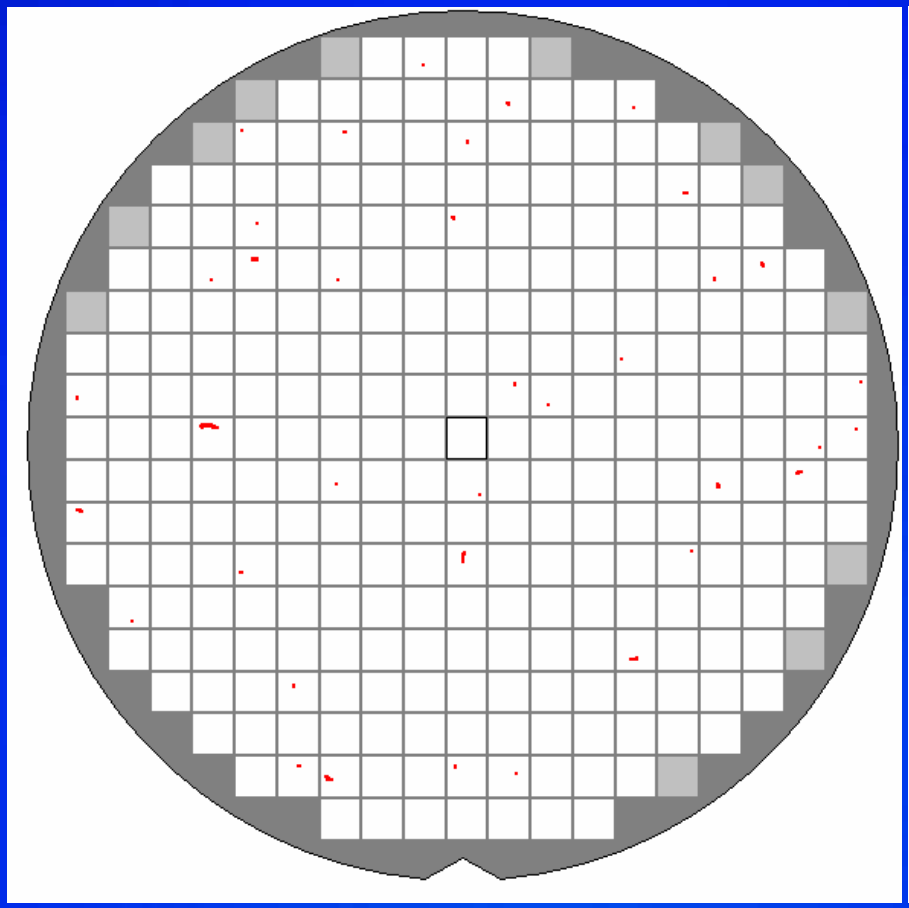


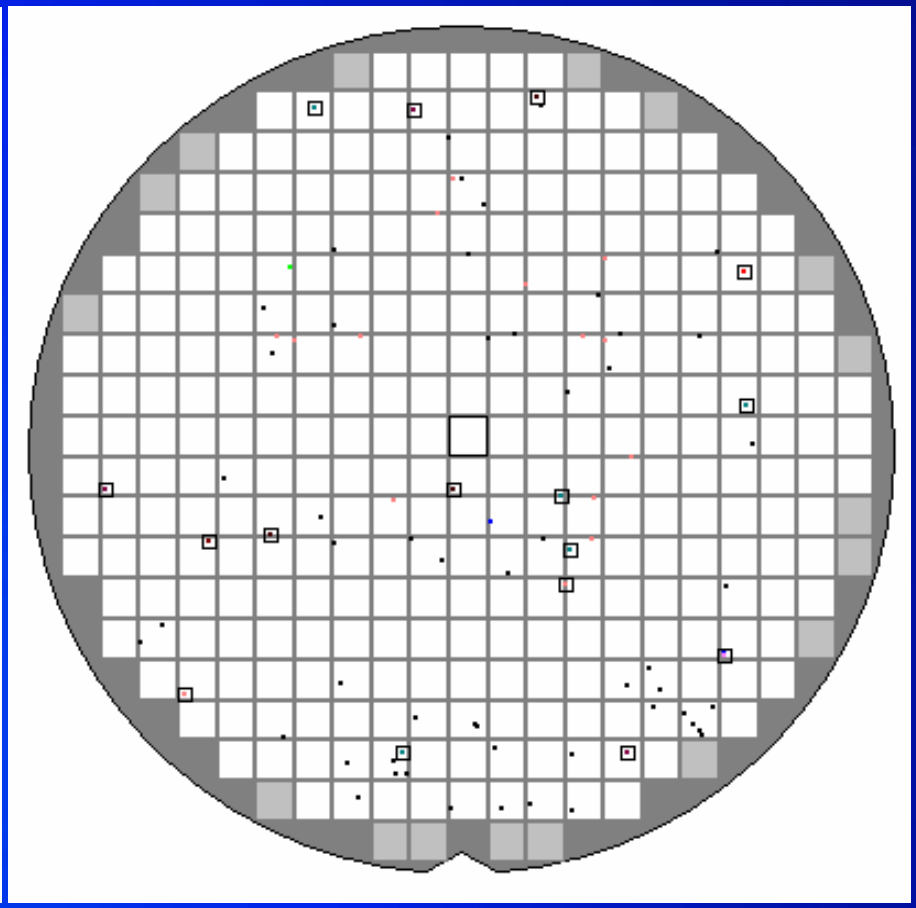
Die size Economics



Will half the die size give you 2X yield?

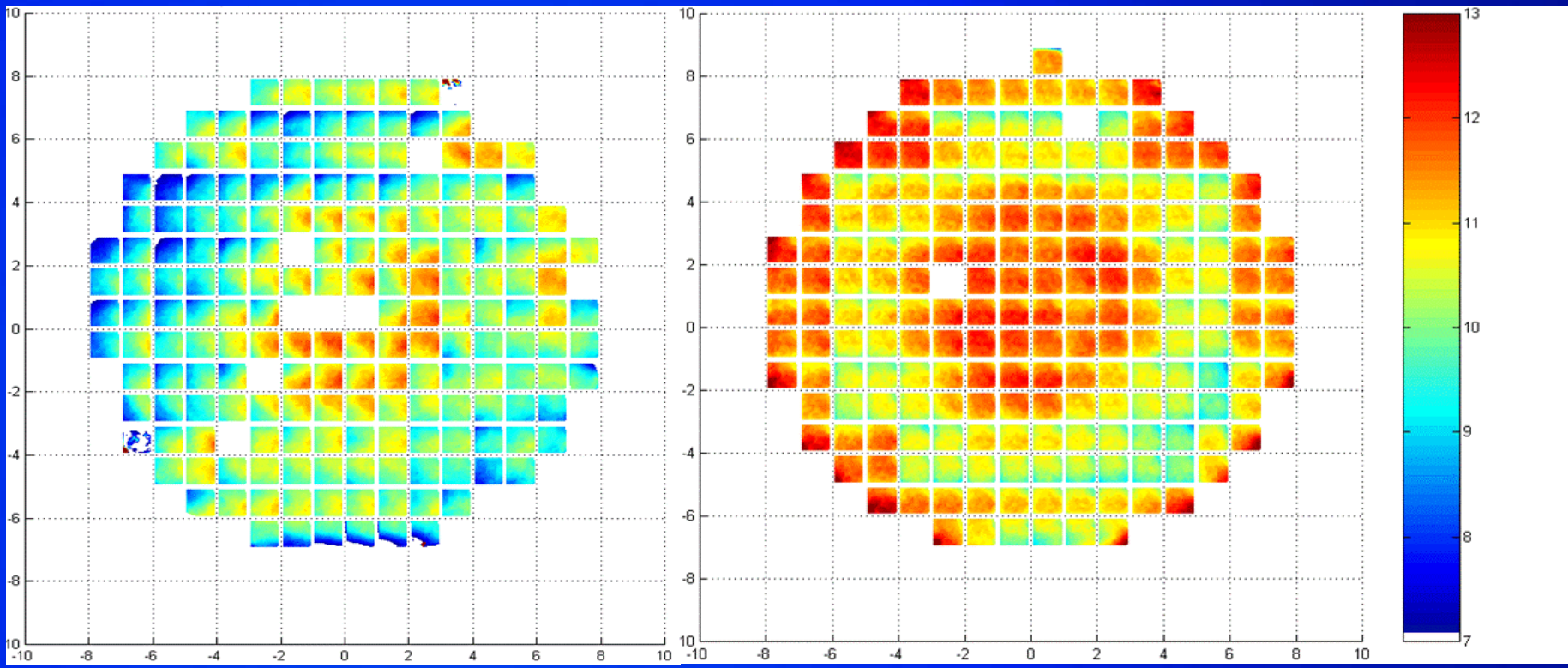
No 2 wafers have the same defect locations





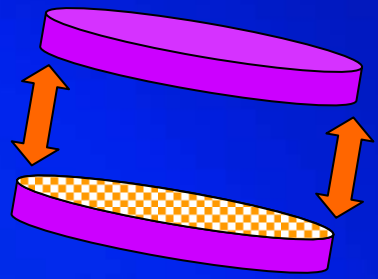
Process variation across wafers

Fast top dies, slow bottom die? What is the result?

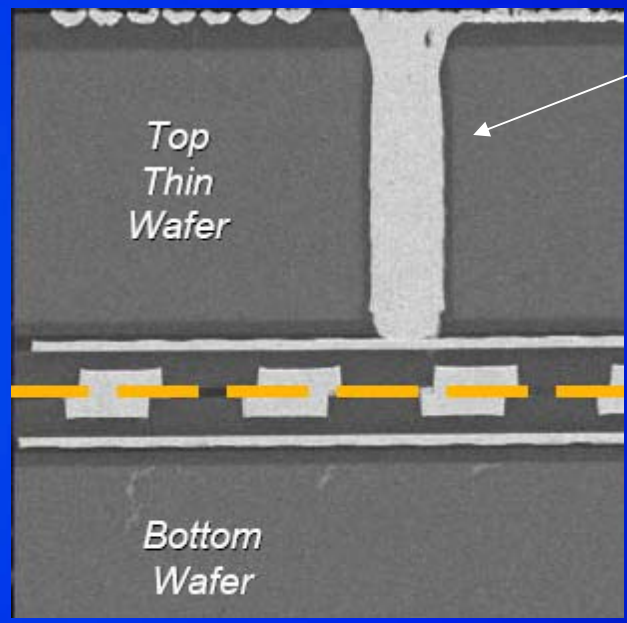


Wafer thinning and stacking

- To stack, you have to thin



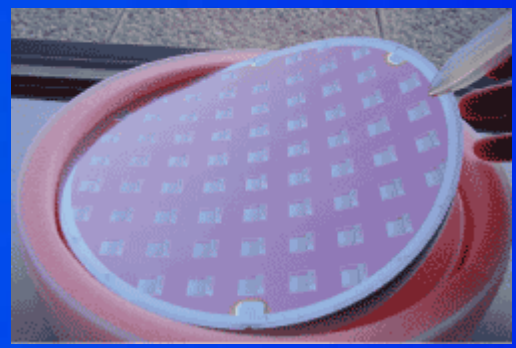
Thin top wafer



Thin layer facilitate via interconnect

Can you dare to probe thinned wafer?

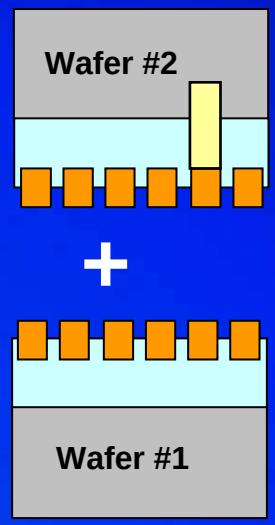
- 2gm of force per probe to ensure good enough electrical contact
  - Translate to 2,000 Kg/sqM force on each pad of a less than 100um silicon film

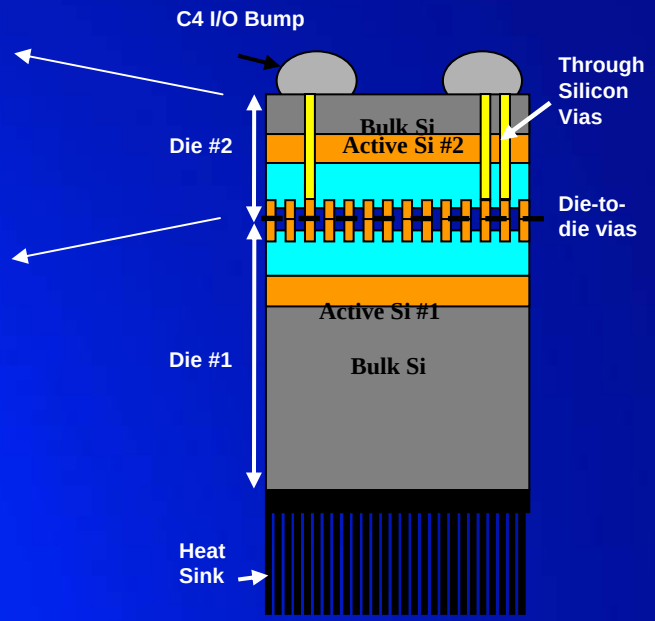


Source: IMEC

Why not probe unthinned wafer?

- All connections to the bottom layers are in buried vias
  - This is where power, gnd and clocks come from
  - Bottom wafer only have tiny connections intended to connect to top wafer only
  - Same problem whether active layers are up or down





The advantage of millions of connections quickly becomes liability

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Challenge?

- This is worse than ***KGD***
  - ***Not a die yet !***
- Testing/Probing of partial circuits with very few connections from the top or bottom side
  - If a full blown infrastructures (thousands of probe pads) are built on top of the either wafer, the advantage will quickly lose appeal

Manufacturing test
can be another hurdle to 3D integration effort

More challenges

- Mixing and matching of top and bottom die require unprecedented process level information collection
  - On a monolithic die, there is no choice; not so when one can select (and match) them
- Thermal, loading at wafer/die level will not be the same when they are sandwiched together
  - Guardbands, margins all take their “taxes”

Can we solve all these problems?

We can’t do it alone.


Let’s create the future together.

Backup

- Turning Chip Design on its Head, Wolfgang Gruber, Synopsys "Compiler" magazine
- 3D packaging issues for ultrasmall systems-in-a-cube, Eric Beyne et. al., *Solid State Technology* April, 2005
- 3D Processing Technology and its Impact on iA32 Microprocessors, Donald Nelson et. al., ICCAD2004
- www.trusi.com
- Through-wafer Via Etching, ANDREW A. CHAMBERS et. al., *Advanced Packaging* April, 2005
- Fabrication and Reliability Issues for Optical Components in Wafer Level Heterogeneous Hyper-Integration, Peter D Persans Sematech Workshop, Oct 25, 2004